the proper section headings required by the Examiner. Additionally, the above amendments to the specification provide the necessary description of elements of the drawings noted by the Examiner as missing from the specification. Please note that element "85" of Figure 21 is already discussed in paragraph [0266]. Additionally, filed on even date herewith is a Request for Approval of Drawing Corrections in which the drawing corrections noted by the Examiner to Figures 1, 2, 6, 7 and 18 are corrected to remove extraneous textural material and provide the proper element "64a" identifier. Consequently, it is respectfully requested that the Examiner's objections to the specification and drawings be withdrawn.

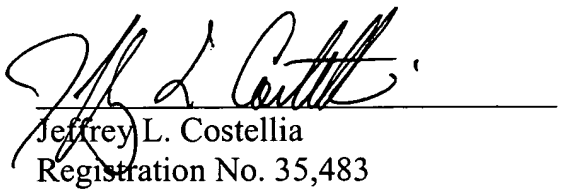
With regard to the Examiner's rejection of claims 1-18, under 35 U.S.C. 102(b), as being anticipated by the teachings of Japanese Patent Application 10-374878 (JP '878), Applicants respectfully traverse that rejection. Initially, the Applicants would point out to the Examiner that the first publication of the JP '878 was not until July 14, 2000 (copy attached). Consequently, since the JP '878 application names the same inventors as the current application, i.e., the JP '878 application is the current application, and since the instant application was filed within one year from the first publication date of the JP '878 application, the JP '878 application is not prior art to the present invention. Therefore, the rejection of claims 1-18, under §102(b), has been made in error and must be withdrawn.

Having responded to all objections and the rejection set forth in the outstanding Office Action, it is submitted that claims 1-18 are in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Lastly, it is noted that a separate Extension of Time Petition (one month) accompanies this response along with a check in payment of the requisite extension

of time fee. However, should that petition become separated from this Amendment, then this Amendment should be construed as containing such a petition. Likewise, any overage or shortage in the required payment should be applied to Deposit Account No. 19-2380 (740756-2063).

Respectfully submitted,



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MARKED UP VERSION

IN THE ABSTRACT

~~[NAME OF DOCUMENT] Abstract~~
~~[ABSTRACT]~~
~~[PURPOSE]~~
~~Providing a semiconductor device with a TFT structure with high reliability~~
~~[MEANS]~~

ABSTRACT OF THE DISCLOSURE

In a CMOS circuit formed on a substrate 100, a subordinate gate wiring line (a first wiring line) 102a and main gate wiring line (a second wiring line) 113a are provided in an n-channel TFT. The LDD regions 107a and 107b overlap the first wiring line 102a and not overlap the second wiring line 113a. Thus, applying a gate voltage to the first wiring line forms the GOLD structure, while not applying forms the LLD structure. In this way, the GOLD structure and the LLD structure can be used appropriately in accordance with the respective specifications required for the circuits.

~~[SELECTED FIGURE] Fig. 1~~

IN THE SPECIFICATION:

Please replace paragraph [0084] with the following

-- [0084] Through this step, a source region 319, a drain region 320, an LDD regions 321a and 321b, and a channel formation region 322 of the NTFT are defined. A drain region 323 and a source region 324 of the PTFT are also doped with phosphorus in this step. However, the P type conductivity thereof can be maintained and is not reversed to the N type conductivity if they are doped with boron in a higher concentration in the previous step. --

Please replace paragraph [0138] with the following

-- [0138] The structure in Fig. 8D is a mode of a pixel matrix circuit. In the structure of Fig. 8D, LDD regions 809 and 810 are provided on either the side closer to the source region or the side closer to the drain region. In other words, no LDD region is provided between two channel formation regions 811 and 812 and the gate wiring layers 808a and 808b. --

Please replace paragraph [0146] with the following

-- [0146] The structure of this embodiment may also be applied to a pixel matrix circuit. The pixel matrix circuit in Fig. 9B uses a single layer of tantalum film for a gate wiring line and employs the above cladding structure, i.e., laminate 902, first conductive layer 902a and second conductive layer 902b, for a part of the gate wiring line that is required to reduce wiring line resistance (a part of the gate wiring line that does not function as a gate electrode). –

ABSTRACT OF THE DISCLOSURE

In a CMOS circuit formed on a substrate 100, a subordinate gate wiring line (a first wiring line) 102a and main gate wiring line (a second wiring line) 113a are provided in an n-channel TFT. The LDD regions 107a and 107b overlap the first wiring line 102a and not overlap the second wiring line 113a. Thus, applying a gate voltage to the first wiring line forms the GOLD structure, while not applying forms the LLD structure. In this way, the GOLD structure and the LLD structure can be used appropriately in accordance with the respective specifications required for the circuits.